HOMEWORK ASSIGNMENT

Q.1) Design 4:1 Mux using Conditional operator.

ANS=

**1)Understanding the Problem:**

In this problem we need to design a 4:1MUX using a conditional operator.In a mux one of the input is selected depending on the select lines.We need to use conditional operator to execute this program.a 4:1 Mux contains 2 select lines,4data ips and a output. Depending on the select line data ip passed will vary.

**2) Devising a Plan/Design:**

In this program we need to just use conditional operator(?:) to execute the design.We may use any type of modeling. In this if select line is 0 output is D0. select line is 1 output is D1 so on.The truth table is as shown:

|  |  |  |
| --- | --- | --- |
| s1 | s0 | output |
| 0 | 0 | D0 |
| 0 | 1 | D1 |
| 1 | 0 | D2 |
| 1 | 1 | D3 |

**3) Carrying out the plan:**

**Verilog code:**

module mux(

input s1,

input s0,

input D0,

input D1,

input D2,

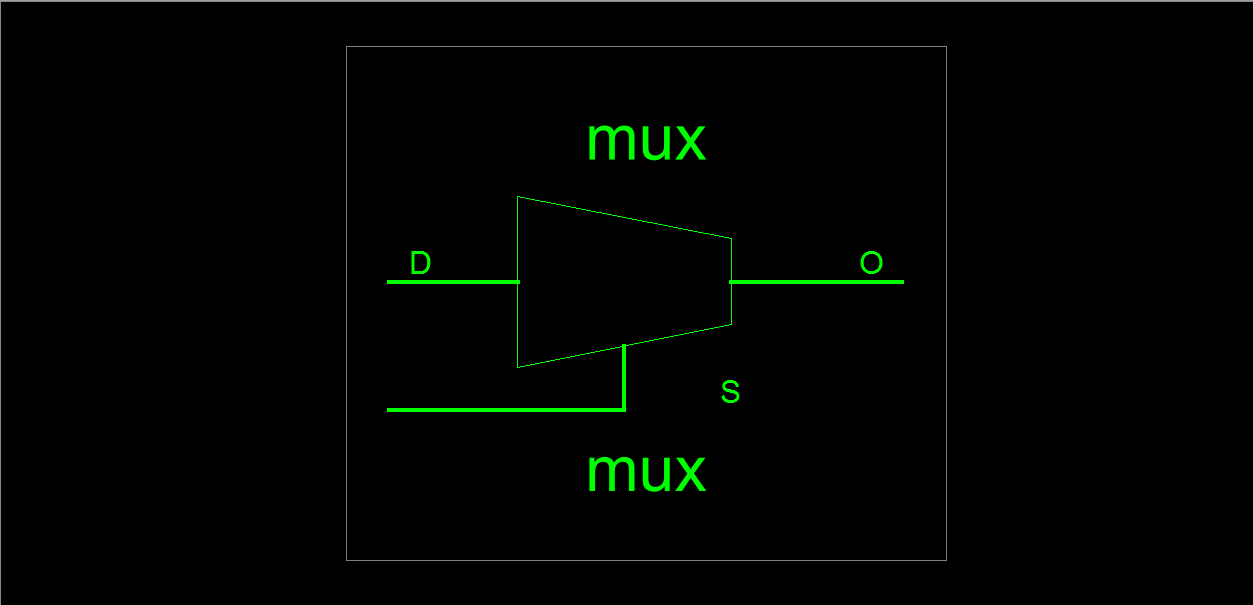
input D3,

output Y

);

assign Y=(s1==1'b0&s0==1'b0)?D0:((s1==1'b0&s0==1'b1)?D1:((s1==1'b1&s0==1'b0)?D2:((s1==1'b1&s0==1'b1)?D3:1'b0)));//code to execute 4:1 MUX using conditional operator

endmodule



**TESTBENCH**

module mux\_tb;

// Inputs

reg s1;

reg s0;

reg D0;

reg D1;

reg D2;

reg D3;

// Outputs

wire Y;

// Instantiate the Unit Under Test (UUT)

mux uut (

.s1(s1),

.s0(s0),

.D0(D0),

.D1(D1),

.D2(D2),

.D3(D3),

.Y(Y)

);

initial begin

// Initialize Inputs

s1 = 0;

s0 = 0;

D0 = 0;

D1 = 0;

D2 = 0;

D3 = 0;

// Wait 100 ns for global reset to finish

#100;

// Add stimulus here

s1=1'b0;

s0=1'b1;

D0=1'b0;

D1=1'b0;

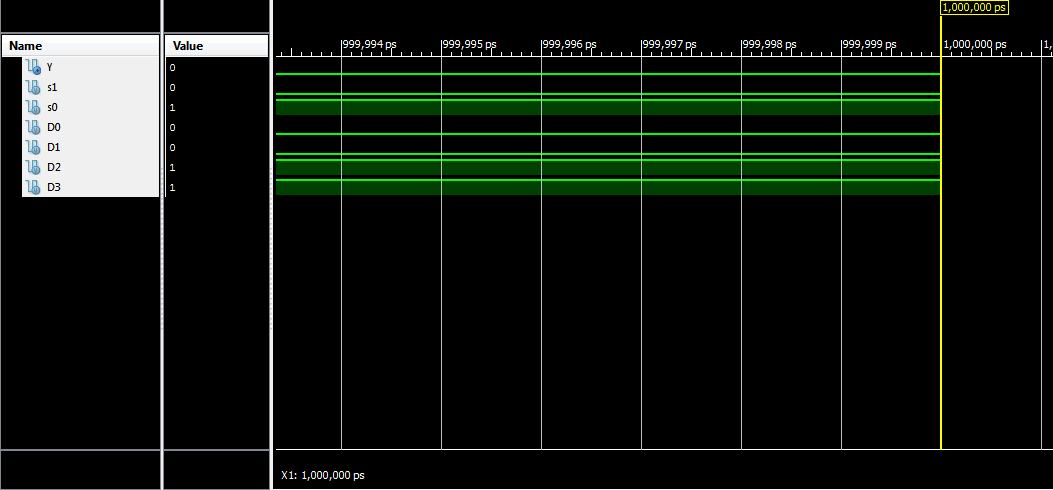
D2=1'b1;

D3=1'b1;

#100;

end

endmodule



**4) Looking back i.e. Self reflection:**

We designed a 4:1 MUX using Conditional Operator..It was verified that the ops of the mux change according to select lines.

**Synthesis report:**

Release 12.1 - xst M.53d (nt)

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--> Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.39 secs

--> Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.39 secs

--> Reading design: mux.prj

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\* Synthesis Options Summary \*

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---- Source Parameters

Input File Name : "mux.prj"

Input Format : mixed

Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "mux"

Output Format : NGC

Target Device : xc3s200-5-pq208

---- Source Options

Top Module Name : mux

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : lut

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Mux Style : Auto

Decoder Extraction : YES

Priority Encoder Extraction : YES

Shift Register Extraction : YES

Logical Shifter Extraction : YES

XOR Collapsing : YES

ROM Style : Auto

Mux Extraction : YES

Resource Sharing : YES

Asynchronous To Synchronous : NO

Multiplier Style : auto

Automatic Register Balancing : No

---- Target Options

Add IO Buffers : YES

Global Maximum Fanout : 500

Add Generic Clock Buffer(BUFG) : 8

Register Duplication : YES

Slice Packing : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Yes

Use Synchronous Set : Yes

Use Synchronous Reset : Yes

Pack IO Registers into IOBs : auto

Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed

Optimization Effort : 1

Library Search Order : mux.lso

Keep Hierarchy : NO

Netlist Hierarchy : as\_optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

Verilog 2001 : YES

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

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\* HDL Compilation \*

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Compiling verilog file "mux.v" in library work

Module <mux> compiled

No errors in compilation

Analysis of file <"mux.prj"> succeeded.

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\* Design Hierarchy Analysis \*

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Analyzing hierarchy for module <mux> in library <work>.

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\* HDL Analysis \*

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Analyzing top module <mux>.

Module <mux> is correct for synthesis.

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\* HDL Synthesis \*

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Performing bidirectional port resolution...

Synthesizing Unit <mux>.

Related source file is "mux.v".

Unit <mux> synthesized.

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HDL Synthesis Report

Found no macro

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\* Advanced HDL Synthesis \*

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Advanced HDL Synthesis Report

Found no macro

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\* Low Level Synthesis \*

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Optimizing unit <mux> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block mux, actual ratio is 0.

Final Macro Processing ...

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Final Register Report

Found no macro

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\* Partition Report \*

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Partition Implementation Status

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No Partitions were found in this design.

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\* Final Report \*

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Final Results

RTL Top Level Output File Name : mux.ngr

Top Level Output File Name : mux

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : NO

Design Statistics

# IOs : 7

Cell Usage :

# BELS : 3

# LUT3 : 2

# MUXF5 : 1

# IO Buffers : 7

# IBUF : 6

# OBUF : 1

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Device utilization summary:

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Selected Device : 3s200pq208-5

Number of Slices: 1 out of 1920 0%

Number of 4 input LUTs: 2 out of 3840 0%

Number of IOs: 7

Number of bonded IOBs: 7 out of 141 4%

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Partition Resource Summary:

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No Partitions were found in this design.

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TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

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No clock signals found in this design

Asynchronous Control Signals Information:

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No asynchronous control signals found in this design

Timing Summary:

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Speed Grade: -5

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 8.138ns

Timing Detail:

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All values displayed in nanoseconds (ns)

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Timing constraint: Default path analysis

Total number of paths / destination ports: 7 / 1

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Delay: 8.138ns (Levels of Logic = 4)

Source: s0 (PAD)

Destination: Y (PAD)

Data Path: s0 to Y

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

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IBUF:I->O 2 0.715 1.040 s0\_IBUF (s0\_IBUF)

LUT3:I0->O 1 0.479 0.000 Y\_F (N5)

MUXF5:I0->O 1 0.314 0.681 Y (Y\_OBUF)

OBUF:I->O 4.909 Y\_OBUF (Y)

----------------------------------------

Total 8.138ns (6.417ns logic, 1.721ns route)

(78.8% logic, 21.2% route)

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Total REAL time to Xst completion: 5.00 secs

Total CPU time to Xst completion: 5.53 secs

-->

Total memory usage is 185976 kilobytes

Number of errors : 0 ( 0 filtered)

Number of warnings : 0 ( 0 filtered)

Number of infos : 0 ( 0 filtered)